#11/a Hawkins 3/29/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Peter Liao; Zsolt G. Takacs		
Assignee:	Cisco Technology Inc.		
Title:	Termination Board For Mounting On Circuit Board		
Serial No.:	09/608,528	Filing Date:	June 30, 2000
Examiner:	Jose H. Alcala	Group Art Unit:	2841
Docket No.:	M-12208 US		

Newport Beach, California
March 14, 2002

BOX AMENDMENT
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

RESPONSE TO OFFICE ACTION

Dear Sir:

This responds to the Office Action mailed on December 14, 2001. Please amend the above-identified application as follows.

IN THE DRAWINGS:

Please amend FIG. 6 to remove the words "Main PCB" and "ASIC" as shown in the attached redline drawing.

IN THE SPECIFICATION:

The following is a clean version of the amended paragraph. In accordance with 37 C.F.R. § 1.121(b)(1)(iii), Attachment B provides marked up versions of the paragraph containing the newly introduced changes.

Please replace the first paragraph on page 1 as follows:

Cross-reference is made to U.S. Patent Application Serial No. 09/481,139, filed January 11, 2000, incorporated herein by reference.

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Please replace the paragraph beginning on page 5, line 19 as follows:

a2

As depicted in Fig. 1, in previous devices a circuit board 112 may have one or more multiple-pin ASICs 114 or similar multi-pin devices mounted thereon. Defining a footprint 115 of the ASIC on the circuit board 112. In many common previous approaches, the underside 116 of the ASIC 114 is provided with an array of solder balls corresponding to ASIC signal, power, ground or other pins. In mounting, the ASIC is positioned such that the solder balls and/or pins are aligned with corresponding pads or the like (only one of which 118 is depicted in Fig. 1). The pads 118 can be provided with printed wires or traces to achieve the desired signal routing, or other electronic connections. In many devices, the array of pins and/or solder balls 122 is relatively dense (such as 1100 or more pins in an area of 1600 mm^2). In many situations, the ball array or pin array is so dense that it is infeasible to position termination resistors within the ASIC footprint 115. In many previous approaches, a printed wire or other lead 124 is provided to connect a pad 118 (coupled to a pin of the ASIC 114), to a termination rsistor 126 which may be positioned outside the footprint 115 and thus may provide a stub having a length 128 sufficiently great to create undesirable effects such as reflection, signal distortion, EMI and the like. These undesirable effects can reach intolerable magnitudes, especially when the ASIC 114 is a high frequency device such as a device with a clock frequency of 1 gigahertz or more.

Please replace the paragraph on page 8, line 6 as follows:

a3

--Fig. 6 illustrates another embodiment of the present invention in which some or all balls 612 of a termination board ball grid array 614 are aligned with vias 616 of the main PCB 618 which receives column columns 622 of a column grid array ASIC 624.--

IN THE CLAIMS:

The following is a clean version of the entire set of pending claims. In accordance with 37 C.F.R. § 1.121(c)(1)(ii), Attachment A provides marked up versions of the claims containing the newly introduced changes. Please amend Claims 1, 3-7, 9 and 11 as follows.

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a4 cont.

1. (Amended) Apparatus for providing termination for at least a first pin of a multi-pin component to be mounted in a footprint area of a first surface of a first circuit board, comprising:

a second circuit board, mounted on a second surface of said first circuit board and providing a connection to at least a first resistance present thereon;

at least a first conductive pathway from said first surface of said first circuit board to a second surface of said first circuit board to provide access for said at least first pin of said multi-pin component to at least a first location of said second circuit board; and

at least a second conductive pathway, formed at least partially through said second circuit board, from said first location of said second circuit board to said at least a first resistance.

2. (As Filed) Apparatus, as claimed in Claim 1, wherein said multi-pin component comprises an ASIC.

3. (Amended) Apparatus, as claimed in Claim 1, wherein said at least a first resistance is positioned on a surface of said second circuit board.

4. (Amended) Apparatus, as claimed in Claim 1, wherein said at least a first resistance is positioned in an interior region of said second circuit board.

5. (Amended) Apparatus, as claimed in Claim 1, wherein said at least a first resistance is selected from among a surface mount resistor, a printed resistance and a buried resistance.

6. (Amended) Apparatus, as claimed in Claim 1, wherein at least a portion of said at least a first conductive pathway comprises a via including a conductive material formed in said first circuit board.

7. (Amended) Apparatus, as claimed in Claim 1, wherein said second circuit board is wholly aligned within at least a portion of the region defined by said footprint.

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8. (As Filed) Apparatus, as claimed in Claim 1, wherein a first portion of said second circuit board is positioned within the region defined by said footprint and a second portion of said second circuit board is positioned within a region outside said footprint.

a4 cncl'd.

9. (Amended) Apparatus, as claimed in Claim 8, wherein said second portion of said second circuit board provides at least a portion of a third conductive pathway to a location of said first circuit board outside said footprint.

10. (As Filed) Apparatus, as claimed in Claim 1, wherein said first pin carries a signal having a frequency greater than about 1 gigahertz.

11. (Amended) Apparatus, as claimed in Claim 1, wherein each of said first and second circuit boards has a thickness and wherein said at least a first conductive pathway and said at least a second conductive pathway have a combined length which is less than the sum of the thickness of said first and second circuit boards.

12. (As Filed) Apparatus, as claimed in Claim 1, wherein said second circuit board is coupled to said first circuit board by a ball grid array.

13. (As Filed) Apparatus, as claimed in Claim 1, wherein said multi-pin component and said second circuit board are coupled to said main circuit board substantially simultaneously.

✓Please Cancel Claims 14-16.

17. (As Filed) Apparatus for providing termination for at least a first pin of a multi-pin component to be mounted in a footprint area of a first surface of a first circuit board, comprising:

board means for providing at least a portion of a first conductive pathway to a resistor, configured for mounting on a second surface of said first circuit board; and

means for providing at least a portion of a second conductive pathway from said first pin to said first conductive pathway.

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REMARKS

Claims 1-13 and 17 are pending. Claims 1, 3-7, 9 and 11 have been amended. Claims 14-16 have been canceled in response to a previous restriction requirement. Applicants request reconsideration and reexamination of the pending claims.

Drawings:

Fig. 6 has been amended to remove superfluous names and acronyms as suggested by the Examiner.

Reference number 666 has not been added to the drawing since the reference number mentioned in the specification was a result of a typographical error which has now been corrected. Accordingly, Applicants request that the objection to the drawings under 37 CFR 1.84(p)(5) be removed.

Reference numbers 128 of Fig. 1 and reference numbers 612 and 616 are now properly mentioned in the specification. Thus, no amendment to the drawings is required. Accordingly, Applicants request that the objection to the drawings under 37 CFR 1.84(p)(5) be removed.

Specification:

The specification has been amended to remove unnecessary reference to attorney file number and to correct incorrect reference numerals and typographical errors. Since each of the Examiner's objections have been addressed, Applicants request any objection to the specification be removed.

Rejection under 35 U.S.C. 112, second paragraph:

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph as being indefinite. For clarity Applicants amend the claims as follows:

Regarding Claim 1, each of the Examiner's assertions regarding the clarity of the claim has been addressed. Accordingly, Claim 1 is in condition for allowance.

Regarding Claims 4, 6, 7, 9 and 11, each of the Examiner's assertions have been addressed. Accordingly, Claims 4, 6, 7, 9 and 11 are in condition for allowance.

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Rejections under 35 U.S.C. 102(a) and 103(a):

Claims 1-3, 6-8, and 10-11 are rejected under 35 U.S.C. 102(a) as being anticipated by Dranchak et al. (USPN 5,953,214). Claims 4, 5, 9, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dranchak et al. Applicants respectfully overcome the rejections as follows.

Claims 1 sets forth, *inter alia*, a second circuit board "providing a connection to at least a first resistance present thereon;" and "at least a second conductive pathway, formed at least partially through said second circuit board, from said first location of said second circuit board to said at least a first resistance." As shown clearly in Applicants' FIG. 2, the second circuit board 226 includes a pathway (232a-232c) to the first resistance (234a-234c) present on the second circuit board. Applicant could find no teaching or suggestion of the features of Claim 1 in Dranchak et al.

The Examiner has characterized substrate 30 of Dranchak et al. as allegedly disclosing the second circuit board of Claim 1. Applicants submit that in contrast to the second circuit board of Claim 1, substrate 30 does not teach or suggest a circuit board providing a connection to a first resistance present thereon. Dranchak et al. discloses that the purpose of second substrate 30 is to help "maintain both the uniform spacing of tails 34 and the uniform height of the top surface of heads 32 over the entire array of second conductors 31." (Dranchak et al., col. 6, lines 28-31)

Accordingly, since Dranchak et al. fails to teach or suggest Applicants invention as set forth in Claim 1, Claim 1 is allowable over Dranchak et al.

Claims 2-13 depend from Claim 1 and are therefore allowable for at least the same reasons as Claim 1, as well as for the novel features which they add.

For example, regarding Claims 3 and 4, Applicants could find no teaching in Dranchak et al. of a second circuit board including a first resistance positioned on "a surface," or an "interior region" of the second circuit board. Regarding Claim 5, Applicants could find no teaching or suggestion in Dranchak et al. of a second circuit board including a first resistance comprising a surface mount resistor, a printed resistance and a buried resistance. Regarding Claim 11, Applicants could find no teaching or suggestion of "at least a first conductive pathway and said at least a second conductive pathway have a combined length which is less than the sum of the thickness of said first and second circuit boards."

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The Examiner has failed to mention Claim 17 in any rejection. Applicants have reviewed Claim 17 in view of Dranchak et al. and submit that Claim 17 is allowable over the cited reference.

CONCLUSION

For the above reasons, pending Claims 1-13 and 17are in condition for allowance and allowance of the application is hereby solicited. If the Examiner has any questions or concerns, a telephone call to the undersigned at (949) 718-5200 is welcomed and encouraged.

EXPRESS MAIL LABEL NO:
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Respectfully submitted,

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